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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/995,319	11/26/2001	Tatsuya Takahashi	81784.0246	9511

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EXAMINER	
AGGARWAL, YOGESH K	

ART UNIT	PAPER NUMBER
2615	

DATE MAILED: 08/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/995,319	TAKAHASHI, TATSUYA	
	Examiner	Art Unit	
	Yogesh K. Aggarwal	2615	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 January 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12 and 16-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12 and 16-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Arguments

1. Applicant's arguments with respect to claims 1-12, 16-20 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-12 are rejected under 35 U.S.C. 102(e) as being anticipated by Kothari et al. (US Patent # 6,552,324).

[Claim 1]

Kothari et al. teaches a charge transfer device having a selectable amplification circuit (figures 2 and 3, also amplifier 33 is depicted in figures 1 and 3), comprising an amplification transistor (M1A, M1B, M2A, M2B) which receives, at a gate, a voltage signal from an output section (figure 1, transfer stage 20) and outputs, from a source, an output signal corresponding to a change in the voltage signal (col. 4 lines 48-51 disclose the current path for the n-devices and p-devices); a load transistor (M3 or M4) connected between the amplification transistor and a first power source (Vdd2) for causing a constant current to flow from the amplification transistor to the side of the first power source (col. 4 lines 35-38); and a control transistor (M9A or M9B or M6A or M7A) connected between the amplification transistor and a second power source (Vdd1), wherein the control transistor controls a current flowing from the second power source

to the amplification transistor according to a control signals (col. 5 lines 30-45, figure 3 wherein the control signals are phiPIX and phiNPIX from an output control circuit 24); and an output control circuit (figure 2, shift register and logic circuitry 24) is connected to a gate of the control transistor M9A and M9B through control signals are phiPIX and phiNPIX for outputting the control signal for reducing a current flowing from the second power source to the amplification transistor during a period in which a pixel signal is not read (col. 5 line 46-col. 6 line 20, col. 1 lines 38-48).

[Claim 2]

The gate of load transistors (M3 or M4) is connected to the same V_{bias} signal (col. 4 lines 42-44) as is the gate of control transistors M6A or M7A.

[Claim 3]

shift register and logic circuitry 24 is connected to a gate of the control transistor M9A and M9B through control signals are phiPIX and phiNPIX and the input terminal and is used for generating control signal and the load transistor will maintain an on state.

[Claim 4]

The symbol for the control transistor (M9A or M9B) shown is for enhancement type.

[Claim 5]

See claim 2.

[Claim 6]

See claim 3.

[Claims 7-12]

These claims correspond to claims 1-6. Therefore they are analyzed and rejected based upon claims 1-6 respectively.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 16-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kothari et al. (US Patent # 6,552,324) in view of Johnson et al. (US Patent # 6,686,957).

[Claims 16 or 17]

Kothari et al. teaches output control means (figure 2, shift register and logic circuitry 24) that control signals are phiPIX and phiNPIX for outputting the control signal for reducing a current flowing from the second power source to the amplification transistor during a period in which a pixel signal is not read (col. 5 line 46-col. 6 line 20, col. 1 lines 38-48) but fails to teach reducing the flow of current while imaging is performed or according to an image quality.

However Johnson et al. teaches a processing system for a CCD or CMOS imaging system having an amplifier 146 (figure 5b) that is subjected to power down performance during a preview mode of operation (col. 6 lines 10-13). Johnson further teaches that the power down is accomplished by switching between a first current level that is half of the second current level from a second power supply PD2 (col. 6 lines 16-21). During power down operation transistors turn off the current from respective amplifier branches (col. 7 lines 40-44). It is noted that during

the preview mode an imaging operation is performed commonly known as video or motion mode. It is well known to one skilled in the art that a video mode correspond to a low quality images and therefore current is reduced to half during an imaging mode and according to image quality as claimed in order to have a power saving that is one half normal operating power subject to a reduced drive level and a corresponding reduced settling time for amplified signals as taught in Johnson (col. 7 lines 50-56).

Therefore taking the combined teachings of Kothari and Johnson, it would have been obvious to one skilled in the art to have been motivated to have reducing the flow of current while imaging is performed or according to an image quality in order to have a power saving that is one half normal operating power subject to a reduced drive level and a corresponding reduced settling time for amplified signals as taught in Johnson (col. 7 lines 50-56).

[Claim 18]

Official Notice is taken that it is notoriously common to have at least one of a horizontal or blanking period as being when a pixel is not read in order to have a high quality image with large number of pixels. Therefore taking the combined teachings of Kothari and Official Notice, it would have been obvious to one skilled in the art to have been motivated to have at least one of a horizontal or blanking period as being when a pixel is not read in order to have a high quality image with large number of pixels.

[Claims 19 and 20]

Kothari et al. teaches a charge transfer device having a selectable amplification circuit (figures 2 and 3, also amplifier 33 is depicted in figures 1 and 3), comprising an amplification transistor (M1A, M1B, M2A, M2B) which receives, at a gate, a voltage signal from an output section

(figure 1, transfer stage 20) and outputs, from a source, an output signal corresponding to a change in the voltage signal (col. 4 lines 48-51 disclose the current path for the n-devices and p-devices); a load transistor (M3 or M4) connected between the amplification transistor and a first power source (Vdd2) for causing a constant current to flow from the amplification transistor to the side of the first power source (col. 4 lines 35-38); and a control transistor (M9A or M9B or M6A or M8A) connected between the amplification transistor and a second power source (Vdd1), wherein the control transistor controls a current flowing from the second power source to the amplification transistor according to a control signals (col. 5 lines 30-45, figure 3 wherein the control signals are phiPIX and phiNPIX from an output control circuit 24); and an output control circuit (figure 2, shift register and logic circuitry 24) is connected to a gate of the control transistor M9A and M9B through control signals are phiPIX and phiNPIX for outputting the control signal for reducing a current flowing from the second power source to the amplification transistor during a period in which a pixel signal is not read (col. 5 line 46-col. 6 line 20, col. 1 lines 38-48).

Kothari et al. teaches output control means (figure 2, shift register and logic circuitry 24) that control signals are phiPIX and phiNPIX for outputting the control signal for reducing a current flowing from the second power source to the amplification transistor during a period in which a pixel signal is not read (col. 5 line 46-col. 6 line 20, col. 1 lines 38-48) but fails to teach reducing the flow of current while imaging is performed or according to an image quality.

However Johnson et al. teaches a processing system for a CCD or CMOS imaging system having an amplifier 146 (figure 5b) that is subjected to power down performance during a preview mode of operation (col. 6 lines 10-13). Johnson further teaches that the power down is

accomplished by switching between a first current level that is half of the second current level from a second power supply PD2 (col. 6 lines 16-21). During power down operation transistors turn off the current from respective amplifier branches (col. 7 lines 40-44). It is noted that during the preview mode an imaging operation is performed commonly known as video or motion mode. It is well known to one skilled in the art that a video mode correspond to a low quality images and therefore current is reduced to half during an imaging mode and according to image quality as claimed in order to have a power saving that is one half normal operating power subject to a reduced drive level and a corresponding reduced settling time for amplified signals as taught in Johnson (col. 7 lines 50-56).

Therefore taking the combined teachings of Kothari and Johnson, it would have been obvious to one skilled in the art to have been motivated to have reducing the flow of current while imaging is performed or according to an image quality in order to have a power saving that is one half normal operating power subject to a reduced drive level and a corresponding reduced settling time for amplified signals as taught in Johnson (col. 7 lines 50-56).

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yogesh K. Aggarwal whose telephone number is (571) 272-7360. The examiner can normally be reached on M-F 9:00AM-5:30PM.

7. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Ometz can be reached on (571)-272-7593. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

8. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

YKA
August 4, 2005

DAVID L. OMETZ
SUPERVISORY PATENT
EXAMINER